MICROCOMPUTER INTERFACE WITH TV

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INTRODUCTION

The cost of CRT monitors justifies an analysis of TV monitor based terminals. The CRT controllers used in the terminal interface are LSI (Large Scale Integration) components and can be programmed for use with TV monitor interface with the microcomputer systems. An important aspect of TV monitors is the need for an external mixer interface circuit while CRT monitors include mixer circuits for producing composite video signals. This paper describes a mixer circuit to implement a TV monitor interface for 8080 based microcomputer systems.

HARDWARE

It consists of a basic computer system, DMA (Direct Memory Access) controller (Intel 8257), CRT controller (8275), Interrupt controller (8259), Octal keyboard, ASCII keyboard, Dot timing logic, Mixer circuit, and a TV monitor (Fig. 1).

The basic system, (Fig. 2), is implemented using an 8080 microprocessor and 4K bytes of memory. The first four pages (256 bytes/page) are implemented with PROM (Programmable Read Only Memory) for utility programs and the following four RAM (Random Access Memory) pages are used for user-oriented programs. The last eight RAM pages are used as display memory. The basic interface functions of the processor are to service the octal keyboard for bootstrapping a user-oriented program in the RAM part of the program memory, to service the ASCII keyboard for loading characters into the display memory, to intialize the peripheral devices, and to reinitialize the DMA controller at the end of every frame of TV display in interrupt mode. The interrupt request lines from the devices are interfaced with an 8259 such that the DMA controller has the top priority. Whenever one or more devices require service, the interrupt controller will resolve the priority, and switch the processor into the appropriate service routine.

Video terminals may utilize either a software display technique (character display) or a hardware controller technique (row display). In the character display technique, the processor is used as a controller eliminating some of the complex interface circuits. The disadvantage of this technique is that the processor is tied up with the display controller operation thereby reducing the data throughput capability of the system. The system described in this paper uses the row display technique (Fig. 3). The basic function of the DMA controller is to put the processor in the HOLD mode and to transfer the display characters from the memory to the CRT controller through the common buses. The operation sequence of the DMA controller is called a DMA cycle and is executed for each display character. The DMA cycle sequence is that when the CRT controller requests data (DRQ), the DMA controller puts the cpu in the HOLD mode, generates the programmed memory address and device select pulses, reads the memory and strobes the display character code into the CRT controller. The MEMR signal drives the MEMR of the memory for reading the data and I/ow signal drives the WR signal of 8275 for strobing the data.

The functions of the 8275 CRT controller include refreshing the TV display by buffering information from display memory and generating horizontal and vertical timing signals for TV synchronization. Visual attribute features allow the implementation of specialized graphic display functions and display enhancement operations. The 8275, having been programmed for a specific screen format, generates a series of DMA (DRQ) request signals which result in the transfer of a row of characters from display memory via the 8275's row buffers. The 8275 presents the character codes to the TV monitor through the dot timing logic and mixer circuits as in Fig. 4. The character code outputs CCO-CC4 are applied to the character generator address line A3-A7. Line count outputs LCO-LC2 from the 8275 are applied to the character generator address lines AO-A2. It should be noted that the 8275 displays character rows one line at a time. The line count outputs

are utilized to determine which line of the character selected by A3-A7 will be displayed. Following the transfer of the first line to the dot timing logic, the line count is incremented and the second line of the character row is selected. The process continues until the last line of the row under consideration is transferred to the dot timing logic. The row by row transfer of character data from display memory to the 8275 continues until the beginning of the last display row. At this time the 8275 issues an interrupt (IRQ) to the 8259. The cpu is then switched into the interrupt service routine to reinitialize the 8257 DMA controller starting address and terminal count parameters. Interrupts are generated by the 8275 every 16.67 ms for a 60HZ screen refresh rate.

One function of the dot timing logic is to transfer display characters synchronously to the TV monitor. Synchronization is achieved by dot and character clocks. These clocks are generated by the processor's clock generator. The dot and character clock frequencies are interrelated and are dependent upon the TV's horizontal oscillator repetition rate and display character width. The clock frequency of the system is 16.81 MHZ and this will fix the dot and character clocks at 8.405 MHZ and 1.2 MHZ respectively as shown in Fig. 4. The display character from the ROM is in parallel mode, whereas the TV monitor requires characters in serial form. The parallel to serial shift register (74166) performs this required mode conversion. The character clock loads the parallel data into the 74166 register and the dot clock shifts the loaded data to the TV monitor. The response time of the 8275 and ROM will be too long to reliably latch the ROM output for the first display character during the first character clock period. This situation is eliminated by introducing the 74175 between the 8275 and the ROM. The 74175 latches the character codes and line counts 1/2 character clock after the positive-going edge of the character clock and loading ROM data into the 74166 shift register on the next positive-going edge of the character clocks. This pipelining technique delays the video output from the shift register by 1 1/2 character clocks, but eliminates the difficulties in sampling the ROM data within the first character clock period.

Due to the video delay associated with the pipelining technique, the dot timing logic delays all the raster signals (HRTC and VRTC) and the video control signals (VSP, RVV, and LTEN) using a two-stage shift register constructed with edge triggered D flip-flops (74175), Fig. 5. The synchronized video signal is then dot-widened by the use of 74LS32 OR-Gates. The contents of display memory may be display or visual and special character codes. The visual attribute characters are classified into character and field attribute types. The display character codes can be used to generate graphic symbols without the use of the character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols as shown in Fig. 6.

The final stage of interfacing is to combine the video signal with the delayed raster timing signals (HRTC and VRTC). This is achieved by means of CMOS analog switches (4066)-based mixer circuit as in Fig. 7. The switch is enabled only when HRTC, VRTC, and DOT widened video are all active. The composite video signal is then connected to the second detector of the TV circuit.

SOFTWARE

The DMA, CRT, and Interrupt controllers are intelligent devices, therefore they must be programmed for the required data communication functions. The device-select-pulses for peripherals are generated by 8205 as shown in Fig. 3.

The device numbers OXH, 1XH, 2XH, 3XH, and 4XH are assigned to 8259, 8275, Octal keyboard, ASCII keyboard, and 8257 respectively. Upon power up, the initialization routine is executed. At the beginning of this routine, the interrupt controller is programmed so that the interrupt traps start with the memory location $000\ 140_8$. The next step in the initialization routine is to program the CRT controller. This begins with a reset command followed by four parameter commands. The parameter commands are for Screen-composition information such as spacing, row length, VRTC length, frame size, position of the underlining, lines per row, and the size of HRTC. The selection of dot clock, HRTC, and the frame size must be within the horizontal repetition rate

(15,970 ± 500 pps) of the TV monitor. For 8.405 MHZ of dot clock, 28 CC1ks (character clocks) of HRTC, 49 characters per row, and a character width of 7 dots, the horizontal oscillator repetition rate is determined as follows:

$$f_{Horiz}=8.405 \times 10^6/((28 \pm 49) \times 7)=15{,}594 \text{ pps.}$$

This value is within the tolerance range of the TV monitor value. The VRTC is programmed to be 2 to satisfy the 60 HZ refresh rate and 24 rows of frame size. The final step in the 8275 programming is to load the cursor position command followed by a start display command. The start display command includes the burst size and burst space for DMA operation.

Finally, the initialization routine blanks the complete display memory, defines intermediate data storage positions for the pointer for display memory and cursor position, enables interrupt, and puts the processor in the halt mode for peripheral interruption. The listings of the initialization and service routines are given in Figs. 8 to 11.

The octal keyboard is used for boot-strapping user programs in object code in the program memory ($004\ 000_8 - 007\ 377_8$). The processor is interrupted and switched into the octal keyboard service routine for every octal key press. The sequence for program loading with the octal keyboard starts with the selection of program location. This is done by the use of H, L, and numeric keys. In the chosen program address, the instructions are stored by the use of numeric and S keys. Instructions are stored one byte at a time and the storage of each byte requires the use of three numeric keys and the storage key, S. At the end of the service routine, the interrupt status prior to the interruption of the processor is re-established.

The DMA refresh routine, Fig. 10, is located at the third page ($002\ 000_8$) of the memory map. In this routine, the interrupt request from 8275 is disabled and the DMA controller is loaded with the address of display memory and the terminal count. The DMA controller is then programmed to be in the autoload mode and the interrupt of 8259 is reset to complete the refresh routine. At the end of every frame of display, the 8275 generates an INTR signal requesting processor interrupt service for DMA refresh. When the INTR signal is active, the 8259 generates an INT signal to switch the processor into the DMA refresh routine. The starting location of program memory is incremented by the number of characters in a row (49) and at the end of every frame as required by the scrolling operation. The DMA refresh routine can be eliminated from the solftware if scrolling operation is not required.

The ASCII keyboard routine, Fig. 11, is located at the second page ($001\ 000_8$) of the memory. It is used for screen control and loading display memory. This routine is serviced by the processor for every ASCII-key press. There are three types of ASCII keys. They are normal display, attribute, and control keys. The control keys are used for screen control operations such as back space, tab, line feed, and escape. These keys do not occupy any character position in the display memory and therefore they are not processed by 8275. These control operations are performed by the processor using dedicated subprograms located at $001\ 134_8$, 001 151g, $001\ 166_8$, and $001\ 047_8$. The normal display codes are loaded in the display memory so that they are displayed under the control of 8275. Attribute keys are classified into field and character codes. The key codes from the encoder of the keyboard are not in standard format and therefore the processor performs code-conversion operation using a look-up table ($001\ 232_8$) before storing these characters in the display memory. A detailed analysis of the ASCII keyboard service routine will reveal that whenever a screen control operation is performed or a code is loaded in the display memory, the cursor position, the character and row counters, and the memory pointer are assigned with the proper value to enable proper screen scrolling operation.

CONCLUSION

A resident assembler can be included in the system with the addition of 4K bytes of memory. Options such as Light Pen Detection and General Attributes can be easily implemented by the addition of simple control logic circuit to the proposed interface. The TV and CRT monitor—based terminals will have identical graphic features if they are implemented with the same monitor controller (8275). The only disadvantage of the TV monitor-based terminals is that they can handle only about 49 characters per row. In applications, hobby market in particular, where the screen size is not a major factor, cost reduction can be achieved by replacing the high cost CRT monitors with the cheaper TV monitors without sacrificing other graphic characteristics.

REFERENCES

Intel Corporation, *Intel 8080 Microcomputer System User's Manual,* Santa Clara, California, 1977.

Hill-burn, J.L., and Julich, P.M. *Microcomputers/Microprocessors: Hardware, Software, and Applications,* Englewood Cliffs, N.J. Prentice Hall, Inc., 1976.

Bruhns, M., *Analysis of Programmable I/O Ports, Northern Illinois University, DeKalb, Illinois, 1980.*

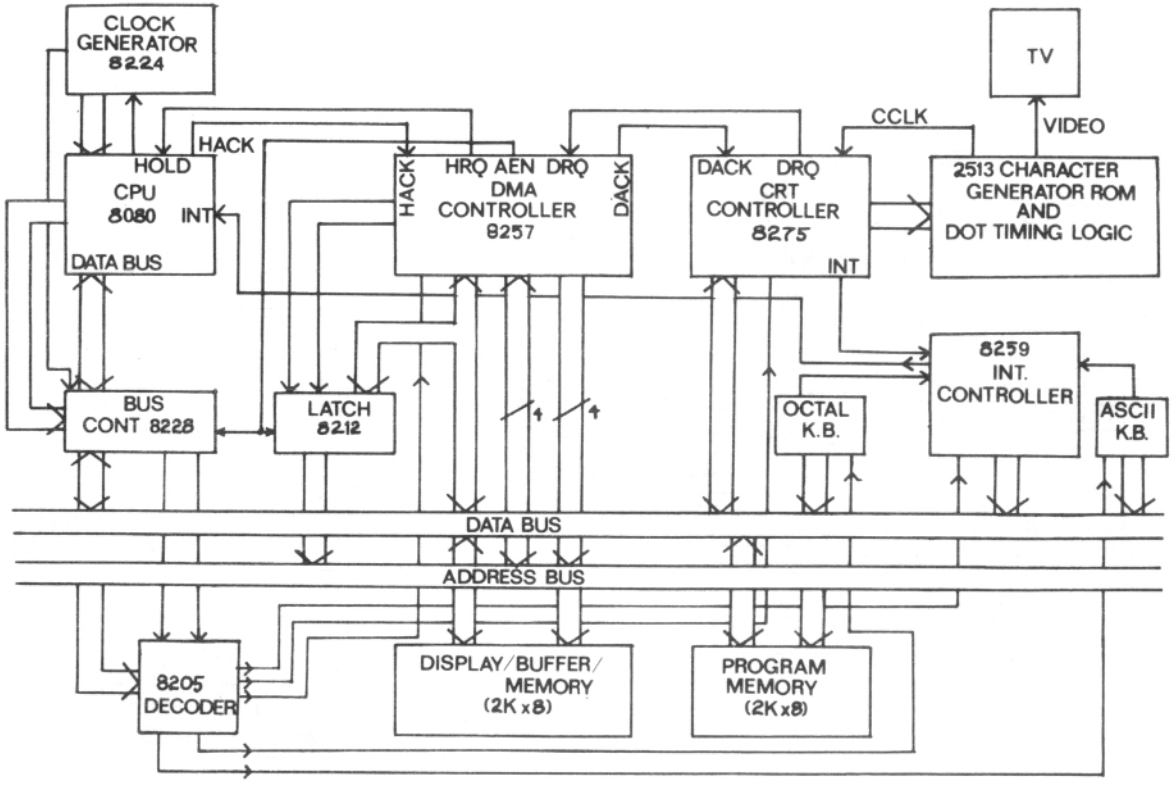

FIG. 1 MICROCOMPUTER SYSTEM – TV MONTOR

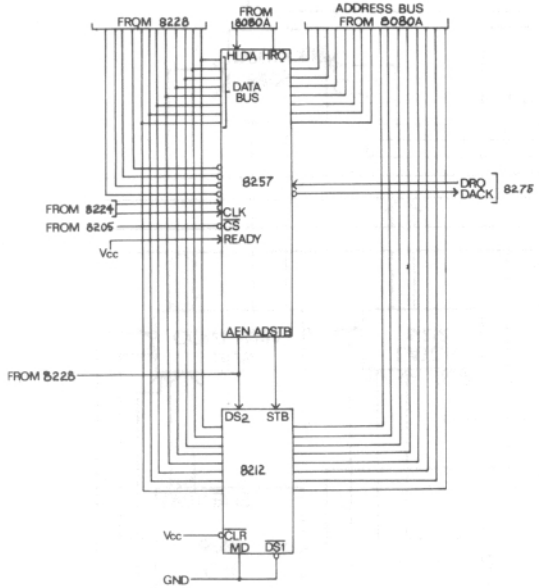

FIG. 2. 8080 BASIC SYSTEM WITH 8257 AND 8259 (CONTD.)

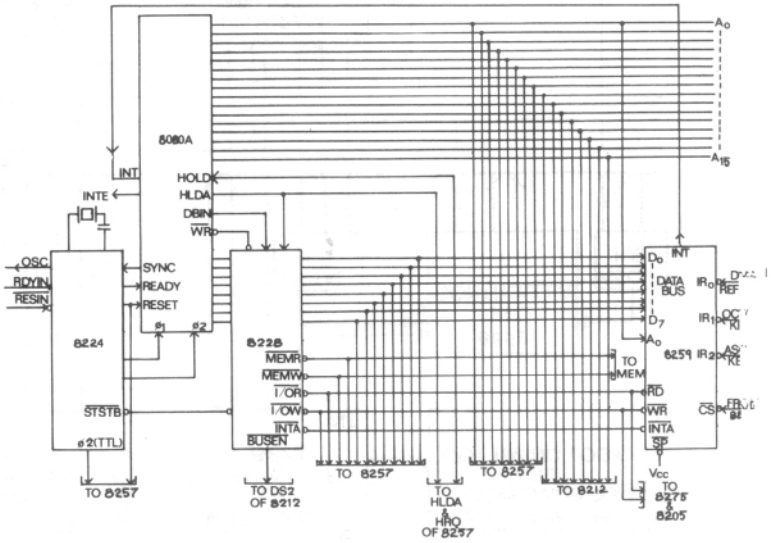

FIG. 2. BASIC SYSTEM WITH 8257 AND 8259

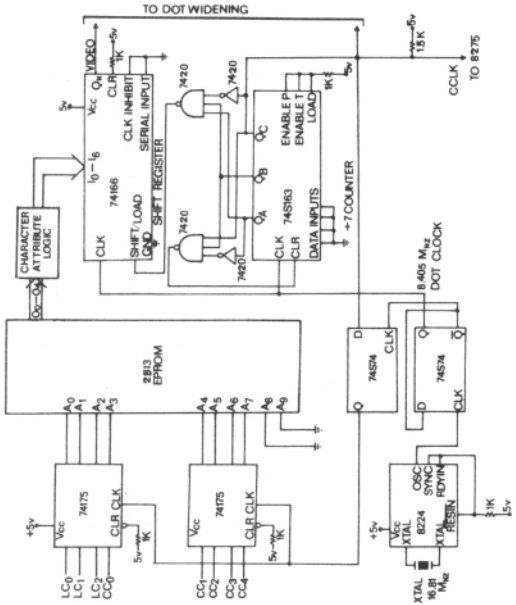

FIG.4 DOT TIMING LOGIC CIRCUIT

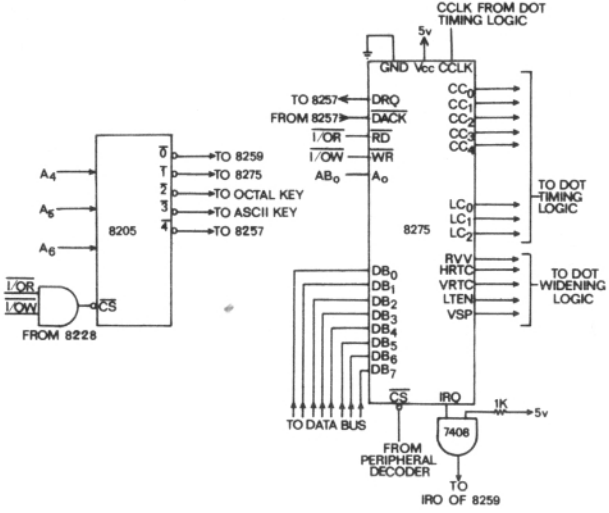

FIG.3 CRT CONTROLLER – PERIPHERAL DECODER DETAILS

FIG. 5 DOT WIDENING CIRCUIT

FIG. 6 CHARACTER ATTRIBUTE LOGIC

```
High 000                                  High 000

Low     Instruction                       Low     Instruction
000     LXI SP                            056     043
001     000                               057     OUT
002     010                               060     11H
003     MVI A; Init. 8259                 061     LXI H; Blank Display Memory
004     166                               062     000
005     OUT                               063     010
006     00H                               064     MVI A
007     MVI A                             065     040
010     000                               066     MOV M,A
011     OUT                               067     INX H
012     01H                               070     MOV A,H
013     MVI A; Init. 8275                 071     CPI
014     000                               072     020
015     OUT; Reset                        073     JNZ
016     X11                               074     064
017     MVI A; Parameters                 075     000
020     060                               076     LXI H     ;Display Memory Pointer
021     OUT                               077     000
022     10H                               100     010
023     MVI A                             101     SHLD
024     127                               102     200
025     OUT                               103     007
026     10H                               104     XCHG
027     MVI A                             105     LXI H     ;Cursor Pointer
030     217                               106     000
031     OUT                               107     000
032     10H                               110     SHLD
033     MVI A                             111     202
034     135                               112     007
035     OUT                               113     EI
036     10H                               114     HLT
037     MVI A; Cursor                     115     JMP
040     200                               116     113
041     OUT                               117     000
042     11H
043     MVI A; Position X                 140     JMP; IRO DMA Refresh
044     000                               141     000
045     OUT                               142     002
046     10H
047     OUT; Position Y                   144     JMP; IR1 Oct. K,B.
050     10H                               145     067
051     MVI A; Preset Counters            146     002
052     340
053     OUT                               150     JMP; IR2 ASCII
054     11H                               151     000
055     MVI A; Start Display              152     001
```

FIG. 8. INITIALIZATION ROUTINE

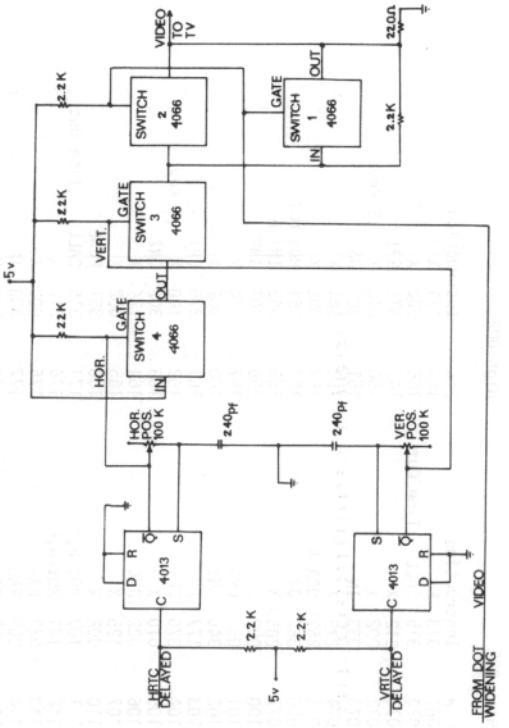

FIG.7 MIXER CIRCUIT WITH CMOS 4066

```
High 002                                  High 002

Low     Instruction                       Low     Instruction
067     373  EI                           145     174  X
070     315  CALL  ;Time Out              146     002  X
071     212  X                            147     376  CPI
072     002  X                            150     010  X    ;S Key
073     333  IN                           151     302  JNZ
074     2XH  X                            152     161  X
075     267  ORA A                        153     002  X
076     362  JP                           154     161  MOV M,C
077     205  X                            155     043  INX H
100     002  X                            156     303  JMP
101     057  CMA                          157     174  X
102     346  ANI                          160     002  X
103     177  X                            161     376  CPI
104     376  CPI                          162     100  X    ;G Key
105     010  X                            163     302  JNZ
106     322  JNC                          164     174  X
107     125  X                            165     002  X
110     002  X                            166     351  PCHL
111     107  MOV B,A                      174     315  CALL   ;Time Out
112     171  MOV A,C                      175     212  X
113     027  RAL                          176     002  X
114     027  RAL                          177     333  IN
115     027  RAL                          200     2XH  X
116     346  ANI                          201     267  ORA A
117     370  X                            202     372  JM
120     260  ORA B                        203     174  X
121     117  MOV C,A                      204     002  X
122     303  JMP                          205     076  MVI A   ;EOI
123     174  X                            206     040  X
124     002  X                            207     323  OUT
125     376  CPI                          210     00H  X
126     020  X    ;L Key                  211     311  RET
127     302  JNZ                          212     365  PUSH PSW    ;Time Out
130     136  X                            213     325  PUSH D
131     002  X                            214     021  LXI D
132     151  MOV L,C                      215     046  X
133     303  JMP                          216     003  X
134     174  X                            217     033  DCX D
135     002  X                            220     172  MOV A,D
136     376  CPI                          221     263  ORA E
137     040  X    ;H Key                  222     302  JNZ
140     302  JNZ                          223     217  X
141     147  X                            224     002  X
142     002  X                            225     321  POP D
143     141  MOV H,C                      226     361  POP PSW
144     303  JMP                          227     311  RET
```

FIG. 9. OCTAL KEYBOARD SERVICE ROUTINE

```
High 002

Low     Instruction
000     365     PUSH PSW
001     345     PUSH H
002     333     IN          ;Reset 8275 Interrupt
003     11H     X
004     076     MVI A
005     000     X           ;Mode Word Reset
006     323     OUT
007     48H     X           ;Command Register Address
010     052     LHLD        ;Start Scroll, Reserve 000 010(8)
011     200     X
012     007     X
013     175     MOV A,L
014     323     OUT         ;Load Low Order in Channel 2
015     44H     X           ;   for Automatic Load
016     174     MOV A,H
017     323     OUT         ;Load High Order in Channel 2
020     44H     X           ;   for Automatic Load
021     076     MVI A       ;Set Terminal Count High Order for
022     227     X           ;49 X 24 Character Display
023     323     OUT
024     45H     X           ;Terminal Count Low Order
025     076     MVI A
026     204     X
027     323     OUT
030     45H     X           ;Terminal Count High Order
031     076     MVI A       ;Start Address Low Order
032     000     X
033     323     OUT         ;Channel 3 Address
034     46H     X
035     076     MVI A
036     010     X           ;Start Address High Order
037     323     OUT
040     46H     X
041     076     MVI A
042     227     X
043     323     OUT
044     47H     X           ;Terminal Count for Channel 3
045     076     MVI A
046     204     X
047     323     OUT
050     47H     X
051     076     MVI A
052     204     X           ;Set Channel 2 Automatic
053     323     OUT
054     48H     X           ;Mode Set
055     076     MVI A
056     040     X           ;End of Interrupt Command
057     323     OUT         ;Reset 8259
060     00H     X           Interrupt
061     341     POP H
062     361     POP PSW
063     373     EI
064     311     RET
```

FIG. 10. DMA REFRESH ROUTINE

```
High 001

Low
000     EI
001     PUSH H
002     PUSH B
003     MVI B
004     032
005     LXI H   ;Table start
006     214
007     001
010     IN      ;ASCII Input
011     3XH
012     NOP
013     NOP
014     CMP M
015     JNZ
016     036
017     001
020     MOV A,L
021     CPI
022     232
023     JNC
024     031
025     001
026     INX H
027     MOV L,M
030     PCHL
031     INX H
032     MOV A,M
033     JMP
034     046
035     001
036     INX H
037     INX H
040     DCR B
041     JNZ
042     014
043     001
044     ANI
045     077
046     STAX D
047     INX D
050     LHLD
051     202
052     007
053     INR H
054     MOV A,H
055     CPI
056     061
057     JNZ
060     110
061     001
062     MVI H
063     000
064     INR L
065     MOV A,L
066     CPI
067     030
070     JNZ
071     110
072     001
073     PUSH H
074     LHLD
075     200
076     007
077     LXI B
100     061
101     000
102     DAD B
103     SHLD
104     200
105     007
```

```
High 001

Low
106     POP H
107     DCR L
110     MVI A   ;Initiate Cursor
                Command
111     200
112     OUT
113     11H
114     MOV A
115     OUT
116     10H
117     MOV A,L
120     OUT
121     10H
122     SHLD
123     202
124     007
125     POP B   ;End of Interrupt
126     POP H
127     MVI A
130     040
131     OUT
132     00H
133     RET
134     LHLD    ;Back Space
135     202
136     007
137     MOV A,H
140     ORA A
141     JZ
142     146
143     001
144     DCX
145     DCR D
146     JMP
147     110
150     001
151     LXI H   ;Escape-Esc
152     000
153     010
154     SHLD
155     202
156     007
157     XCHG
160     LXI H
161     000
162     000
163     JMP
164     110
165     001
166     LXI H   ;Line Feed
167     061
170     000
171     DAD D
172     XCHG
173     LHLD
174     202
175     007
176     JMP
177     064
200     001
214     BS  210  ;Special Key Table
215     X   134
216     TAB 011
217     X   047
220     LF  012
221     X   166
222     NOP 000
223     NOP 000
224     ESC 033
225     X   151
```

```
High 001

Low
232     A                   201   ;Field Attributes
233     X   RVV             220
234     B                   202
235     X   BLINK           202
236     C                   003
237     X   UND. LINE       240
240     D                   204
241     X   B + C           242
242     E                   005
243     X   A + B           222
244     F                   006
245     X   A + C           260
246     G                   207
247     X   A + B + C       262
250     K                   213
251     X   ⌐               300   ;Character Attributes
252     L                   014
253     X   ¬               304
254     N                   216
255     X   L               310
256     O                   017
257     X   ⌋               314
260     Q                   021
261     X   ⊤               320
262     R                   022
263     X   ⊣               324
264     S                   223
265     X   ⊢               330
266     T                   024
267     X   ⊥               334
270     U                   225
271     X   —               340
272     V                   226
273     X   |               344
274     W                   027
275     X   +               350
276     DEL                 237
277     X                   200
```

FIG. 11. ASCII KEYBOARD SERVICE ROUTINE